REMARKS

Claims 1-32 are pending in the application. Claims 1-32 have been examined. Claims 1-2, 5-16, 20, 22-25, 27-28 and 30-32 are rejected and claims 3-4, 17-19, 21, 26, and 29 are allowable. Claims 1-3, 5-7, 9-11, 13-17, and 19-32 have been amended to more clearly define the invention. Reconsideration and allowance of the claims are respectfully requested.

THE SPECIFICATION

The specification is objected to because the information in the "cross-references to related applications" section is not up to date. This section has been updated as shown above.

THE CLAIMS

Allowable Claims 3-4, 17-19, 21, 26 and 29

Applicants note with appreciation the indication of allowable claims 3-4, 17-19, 21, 26, and 29. Claims 3, 17, 21, 26, and 29 have each been amended to include the limitations of their base claims. Claims 4 is dependent on claim 3, and claims 18-19 are dependent on claim 17.

Rejection Under 35 U.S.C. §112

Claims 9-12 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. More specifically, claim 9 is rejected because the limitations "the first range of values" in line 16 and "the second range of values" in line 18 lack antecedent basis. Claims 10-12 are similarly rejected because they are dependent on claim 9.

For claim 9, the limitations "a first range of values" in given in line 8 and "a second range of values" is given in line 10. Antecedent basis is thus provided for the limitations "the first range of values" in line 16 and "the second range of values" in line 18. The rejection of claims 9-12 under 35 U.S.C. §112, second paragraph, should thus be withdrawn.

Rejection of Claims 1-2, 5-7, 20, 22-24, 27-28, and 30-32 Under 35 U.S.C. §102(b)

Claims 1-2, 5-7, 20, 22-24, 27-28, and 30-32 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hirose *et al.* (U.S. Patent No. 4,839,846). The rejection states that Hirose discloses a floating-point unit configurable to perform floating-point operations in FIGS. 7-8. The floating-point unit receives and processes one or more input operands (60) to provide a preliminary result (70), determines whether the preliminary result falls within one of a plurality of ranges of values (based on the least significant bits in FIG. 4A), and sets the preliminary result to one of a plurality of set values if the preliminary result falls within one of the plurality of ranges of values (col. 2, lines 35-48).

Hirose Reference

Hirose describes in FIG. 8 a method of performing floating-point add/subtract operation by the floating-point unit in FIG. 7 (see col. 3, lines 9-10). For a floating-point add/subtract operation, the difference between the exponents of two operands is first determined (60), the mantissa of the smaller operand is shifted to the right by the difference between the exponents, and the two mantissas are added or subtracted (70) (see col. 2, lines 34-38). The result of the add/subtract operation may be a number that is not normalized. The operation result is thus normalized and then rounded. The normalization is performed by shifting the mantissa to the left so that the most significant bit (MSB) of the mantissa is a one ('1') and decrementing the exponent accordingly. The rounding is performed based on (a) the least significant bit (LSB) of the mantissa after the normalization, (b) three bits to the right of the LSB (which are referred to as the "guard" bit, "round" bit, and "sticky" bit, as shown in FIG. 3), and (c) the rounding mode selected for use. Four different rounding modes are given in FIGS. 4A through 4D. Whether or not the mantissa should be rounded up is determined based on these four mantissa bits and the selected rounding mode. If a round-up is performed, an overflow in the mantissa may occur, as shown in FIG. 16C. In this case, the mantissa is shifted right by one bit to obtain a normalized mantissa, as shown in FIG. 16D, and the exponent is incremented by one (see col. 4, lines 65-68).

Present Invention

Claim 1 of the present invention, as amended, recites:

"A floating-point unit (FPU) configurable to perform floating-point operations, comprising:

an operand processing section operative to, for each floating-point operation, receive and process one or more input operands to provide a preliminary result comprised of a mantissa and an exponent; and

an operand flush section coupled to the operand processing section and operative to

determine whether the preliminary result falls within one of a plurality of ranges of values between zero and a minimum normalized floating-point number, a_{min}, and

set the preliminary result to one of a plurality of set values if the preliminary result falls within one of the plurality of ranges of values."

Applicants submit that claim 1 is not anticipated by Hirose for at least the following reasons.

First, Hirose does not describe nor suggest an operand flush section operative to "determine whether the preliminary result [which is comprised of a mantissa and an exponent] falls within one of a plurality of ranges of values between zero and a minimum normalized floating-point number." The section of Hirose indicated as disclosing this feature (FIG. 4A) actually describes the checking of a sign bit and four bits of the mantissa to determine whether or not to round up. Checking these five bits alone cannot determine whether the preliminary result falls within one of a plurality of ranges of values between zero and a minimum normalized floating-point number.

Second, Hirose does not describe nor suggest the operand flush section operative to "set the preliminary result to one of a plurality of set values if the preliminary result falls within one of the plurality of ranges of values." The section of Hirose indicated as disclosing this feature (col. 2, lines 35-48) actually describes a floating-point add/subtract operation, which includes add/subtract of the operand, normalization of the operation result, and rounding after the normalization.

For at least the above reasons, Applicants submit that claim 1 of the present invention is not anticipated by Hirose.

Independent claims 20, 23, 27, and 30-32 each recite features similar to that described above for claim 1. Applicants submit that these independent claims are not anticipated by Hirose for reasons similar to those noted above for claim 1.

Claims 2 and 5-7 are dependent on claim 1, claim 22 is dependent on claim 20, claim 24 is dependent on claim 23, and claim 28 is dependent on claim 27. These claims are not anticipated by Hirose for at least the reasons noted above for their base claims. These dependent claims may further recite additional features not described

or suggested by Hirose. For example, Hirose does not describe nor suggest "set the preliminary result to one of two set values if it falls within one of two ranges of values" (claim 2). Instead, Hirose performs normalization, rounding, and normalization (if necessary) for the result of floating-point add/subtraction operation. Hirose also does not describe nor suggest "determination of whether the preliminary result falls within one of the ranges can be performed by checking an exponent of the preliminary result" (claim 5, and similarly in claims 22, 24, 28). In contrast, Hirose checks the sign bit and the mantissa bits to determine whether or not to round up (see FIGS. 4A-4D).

Accordingly, the §102(b) rejection of claims 1-2, 5-7, 20, 22-24, 27-28, and 30-32 should be withdrawn.

Rejection of Claim 16 Under 35 U.S.C. §102(b)

Claim 16 stands rejected under 35 U.S.C. §102(b) as being anticipated by Elliott *et al.* (U.S. Patent No. 5,553,015). The rejection states that Elliott discloses a floating-point unit configurable to perform arithmetic operations (abstract) and including (1) an exponent processing section (**107** and **109**) operative to receive and process one or more exponents for one or more input operands to provide a preliminary result exponent and (2) an exponent flush unit (**109**, **111**, **113**, **115**, and **117**) operative to receive and compare the preliminary result exponent to at least one exponent comparison value (**105**) and set the preliminary result exponent to one of a set of possible exponent set values based on results of the comparison.

Elliott Reference

Elliott describes in FIG. 3 a circuit for detecting out of range conditions for a floating-point exponent result (i.e., underflow and overflow of the exponent result) and which can operate concurrently with another unit that computes this floating-point exponent result. The circuit sums (a) an intermediate exponent for the two operands of a floating-point add/subtract operation, (b) an exponent adjust value for the number of left shifts of the mantissa result of the floating-point operation (to normalize the result), and (c) one of four different exponent range check values (+1022, -1023, +126, and -127). The output of the circuit is used to determine whether the floating-point exponent result underflow (is too small) or overflow (is too large) for single-precision with an exponent range of -126 to +127 and double-precision with an exponent range of -1022 to +1023.

Present Invention

Claim 16 of the present invention, as amended, recites:

"A floating-point unit (FPU) configurable to perform arithmetic operations, comprising:

an exponent processing unit operative to receive and process one or more exponents for one or more input operands for each arithmetic operation to provide a preliminary result exponent partially indicative of a result of an arithmetic operation; and

an exponent flush unit coupled to the exponent processing unit, the exponent flush unit operative to

receive and compare the preliminary result exponent to at least one exponent comparison value greater than zero and less than an exponent value, E_{min}, for a minimum normalized floating-point number, and

set the preliminary result exponent to one of a plurality of exponent set values based on results of the comparison between the preliminary result exponent and the at least one exponent comparison value."

Applicants submit that claim 16 is not anticipated by Elliott for at least the following reasons.

First, Elliott does not describe nor suggest "compare the preliminary result exponent to at least one exponent comparison value greater than zero and less than an exponent value, E_{min}, for a minimum normalized floating-point number."

Instead, Elliott uses exponent range check values of +127 and +1022 to detect for underflow of the minimum exponent values of -127 and -1023, respectively, and exponent range check values of -126 and -1023 to detect for underflow of the minimum exponent values of +126 and +1023, respectively.

Second, Elliott does not describe nor suggest "set the preliminary result exponent to one of a plurality of exponent set values." Rather, the circuit in FIG. 3 of Elliott only provides indications for underflow and overflow (i.e., whether or not there is an underflow or overflow of the result). In this regard, the circuit in FIG. 3 of Elliott may be equivalent to underflow/overflow prediction unit **712** shown in FIG. 7 of the present invention, and is NOT equivalent to the exponent flush unit **716** in FIG. 7, which is recited in claim 16.

For at least the above reasons, Applicants submit that claim 16 of the present invention is not anticipated by Elliott. The §102(b) rejection of claim 16 should be withdrawn.

Rejection of Claim 8 Under 35 U.S.C. §103(a)

Claim 8 stand rejected under 35 U.S.C. §103(a) as being obvious over Hirose *et al.* (U.S. Patent No. 4,839,846). The rejection states that the features of base claim 1 are disclosed by Hirose and the additional limitation in claim 8 is obvious.

Applicants submit that claim 1 is not anticipated by Hirose for the reasons noted above. Thus, Hirose cannot be used as the basis of the §103(a) rejection of claim 8, which is dependent on claim 1. The §103(a) rejection of claim 8 should be withdrawn.

Rejection of Claims 9, 11-15 and 25 Under 35 U.S.C. §103(a)

Claim 9, 11-15 and 25 stand rejected under 35 U.S.C. §103(a) as being obvious over Hirose *et al.* (U.S. Patent No. 4,839,846) in view of Mansingh (U.S. Patent No. 6,199,089). With regard to claim 9, the rejection states that Hirose discloses the mantissa processing section and Mansingh in FIG. 3A discloses the exponent processing section. The rejection further states that unit **208** in FIG. 3A of Mansingh sets the preliminary result exponent to first or second exponent values if the result of a floating-point operation falls within first and second ranges of value.

Mansingh Reference

Mansingh describes in FIG. 3A a floating-point unit **100** with two operation units **200** and **300** (see FIG. 1). Operation unit **200** is used to perform addition or subtraction when the absolute value of the difference between the exponents of the two operands is greater than one (col. 2, lines 62-66). Operation unit **300** is used to perform subtraction when the absolute value of the exponent difference is less than or equal to one (col. 3, lines1-4)). Decision unit **208** determines whether (a) the absolute value of the exponent difference is less than or equal to one ('yes' from unit **208**) in which case operation unit **300** is used or (b) the absolute value of the exponent difference is greater than one ('no from unit **208**) in which case operation unit **200** is used.

Present Invention

Claim 9 of the present invention, as amended, recites:

"A floating-point unit (FPU) configurable to perform floating-point operations, comprising:

a mantissa processing section operative to, for each floating-point operation,

receive and process one or more mantissas for one or more input operands to provide a preliminary result mantissa,

set the preliminary result mantissa to a first mantissa value if a result of a floating-point operation, comprised of a mantissa and an exponent, is within a first range of values between zero and a minimum normalized floating-point number, a_{min}, and

set the preliminary result mantissa to a second mantissa value if the result is within a second range of values between zero and the minimum normalized floating-point number, a_{min}; and

an exponent processing section coupled to the mantissa processing unit and operative to

receive and process one or more exponents for the one or more input operands to provide a preliminary result exponent,

set the preliminary result exponent to a first exponent value if the result is within the first range of values, and

set the preliminary result exponent to a second exponent value if the result is within the second range of values."

Applicants submit that claim 9 is patentable over Hirose in view of Mansingh for at least the following reasons.

First, Mansingh does not describe nor suggest determination of whether "a result of a floating-point operation, comprised of a mantissa and an exponent, is within a first range of values between zero and a minimum normalized floating-point number." Instead, decision unit **208** of Mansingh determines whether the absolute difference between the exponents of two operands is (a) greater than one or (b) less than or equal to one. Second, Mansingh does not describe nor suggest "set the preliminary result exponent to a first exponent value if the result is within the first range of values." Rather, the output from decision unit **208** is a control signal that indicates whether to use operation unit **200** or **300**. Third, Hirose does not describe nor suggest "set the preliminary result mantissa to a first mantissa value if a result of the floating-point operation is within a first range of values," as described below.

For at least the above reasons, Applicants submit that claim 9 of the present invention is patentable over Hirose in view of Mansingh.

Independent claim 13 recites features similar to that described above for claim 9 and is patentable for reasons similar to those noted above for claim 9. Claims 11-12 are dependent on claim 9, claims 14-15 are dependent on claim 13, and claim 25 is

dependent on claim 23. These claims are patentable over Hirose in view of Mansingh for at least the reasons noted above for their base claims.

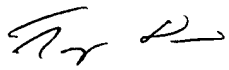
Accordingly, the §103(a) rejection of claims 9, 11-15 and 25 should be withdrawn.

CONCLUSION

Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 289-0600.

Respectfully submitted,



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